IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Applicant(s): M. Calle et al.
Case: 10-6-2
Serial No.: 10/029,705
Filing Date: December 21, 2001
Group: 2665
Examiner: Cynthia L. Davis

I hereby certify that this paper is being deposited on this date with the U.S. Postal Service as first class mail addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Signature: _____ Date: February 8, 2006

Title: Method and Apparatus for Classification of Packet Data Prior to Storage in Processor Buffer Memory

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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants hereby request review of the final rejection in the above-identified application. A Notice of Appeal is filed concurrently herewith. The review is requested for the reason(s) stated in the Remarks section below.

REMARKS

The present application was filed on December 21, 2001 with claims 1-17. Claims 1-17 remain pending. Claims 1 and 17 are the independent claims.

Claims 1-6, 9, 11-15 and 17 stand rejected under 35 U.S.C §102(e) as being anticipated by U.S. Patent No. 6,724,767 (hereinafter "Chong"). The remaining claims stand rejected under 35 U.S.C. §103(a) over Chong alone or in combination with other cited references.

Applicants respectfully traverse the §102(e) and §103(a) rejections.

With regard to the §102(e) rejection, Applicants initially note that MPEP §2131 specifies that a given claim is anticipated "only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference," citing Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Moreover, MPEP §2131 indicates that the cited reference must show the "identical invention . . . in as complete detail as is contained in the . . . claim," citing Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). For the reasons identified below, Applicants submit that the Examiner has failed to establish a *prima facie* case of anticipation of claims 1-6, 9, 11-15 and 17 by Chong.

Independent claims 1 and 17 recite first and second classification circuitry which perform respective first pass and second pass classifications on portions of a given packet. The portion of the given packet that is subject to second pass classification is determined by the first pass classification. Such an arrangement provides significant advantages in terms of reducing the required amount of buffer memory. See the specification at, for example, page 6, lines 20-22.

It is believed that Chong fails to teach or suggest the claimed arrangements, and fails to provide their associated memory reduction advantages.

In formulating the §102(e) rejection, the Examiner relies on the receiver block 60 as described in column 6, lines 17-19, of Chong. See the final Office Action at page 3, first paragraph, lines 1-10. However, this disclosure from Chong simply indicates that, in an ATM termination mode of operation, receiver block 60 "upon cell arrival . . . extracts the cell header and passes the cell payload to either an internal cell buffer or local memory." This appears to be nothing more than conventional processing of ATM cells to separate the header and payload portions of the cells. Chong does not make any mention at all regarding performance of both a

first pass classification and a second pass classification, much less specify a particular relationship between first pass and second pass classification such as that recited in claims 1 and 17.

In an amendment filed October 12, 2005, Applicants made the foregoing arguments and also amended claims 1 and 17 to indicate that the first classification circuitry in processing a plurality of packets comprising the given packet and an additional packet generates respective first and second first pass classification determinations that are different from one another and that result in different-sized portions of the respective packets being stored in the second memory circuitry for processing by the second classification circuitry. Thus, it is clear that the claimed arrangements provide an ability to alter, from one packet to another packet, the particular packet portions that are stored in the second memory circuitry. As noted above, this advantageously allows a significant reduction in the size of the second memory circuitry. See the specification at, for example, page 6, lines 20-22. Simply removing cell headers for all received cells as recited in Chong does not provide such an advantage.

Support for these previously-entered amendments can be found in the specification at, for example, page 4, line 21, to page 5, line 2, page 6, lines 12-22, page 7, lines 16-18, and page 10, lines 12-14.

In the final Office Action, the Examiner argues that the added limitations are shown in Chong at column 6, lines 19-21. See the final Office Action at page 3, first paragraph, lines 10-17. However, this relied-upon portion of Chong simply indicates that the receiver block 60 utilizes the extracted cell header to form a VC descriptor address, and then uses the VC descriptor address to fetch a VC descriptor. See also column 5, lines 42-44, of Chong. These teachings do not disclose or suggest the claimed arrangements in which different first pass classification determinations are generated for different packets, resulting in different-sized portions of the different packets being stored in a particular memory for processing by second pass classification circuitry. Instead, Chong simply indicates that for each received ATM cell, the cell header is extracted and the cell payload is passed to either an internal cell buffer or local memory. See Chong at column 6, lines 16-19. As is well known, ATM cells are fixed rather than variable in size. More specifically, each ATM cell is 53 bytes in length, with a 5-byte header and 48-byte payload. Thus, for each ATM cell processed by the receiver block 60, the 5-

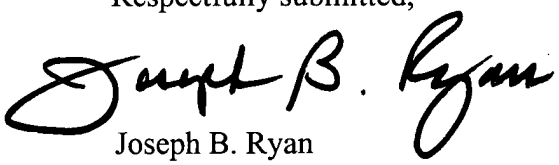
byte header is extracted and the 48-byte payload is stored in an internal cell buffer or local memory. Accordingly, Chong clearly fails to meet the limitations of claims 1 and 17 as previously amended.

Applicants therefore respectfully submit that a proper *prima facie* case of anticipation of claims 1-6, 9, 11-15 and 17 has not been established. The §102(e) rejection is believed to be improper, and should be withdrawn.

With regard to the §103(a) rejections, the additional references fail to supplement the above-noted fundamental deficiencies of Chong as applied to the independent claims. The §103(a) rejections are therefore also believed to be improper and should be withdrawn.

In view of the above, Applicants believe that claims 1-17 are in condition for allowance, and respectfully request the withdrawal of the §102(e) and §103(a) rejections.

Respectfully submitted,



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